What is claimed is:

1. A method for forming a metal-insulator-metal ("MIM") capacitor comprising the steps of:

forming a first metal film and an dielectric film on a semiconductor substrate;

patterning the dielectric film to form a trench through which the first metal film is exposed;

forming an insulation film and a second metal film on a surface of the trench and the dielectric film;

providing a mask pattern defining a capacitor forming area on the second metal film;

forming an upper electrode by etching the second metal film and the insulation film by using the mask pattern and the dielectric film as an etching barrier and an etching stopper layer, respectively;

removing the mask pattern; and

forming a lower electrode by patterning the dielectric film and the first metal film.

2. The method of claim 1, wherein said dielectric film comprises an oxide film or nitride film.

3. The method of claim 1, wherein a thickness of said insulation film is about 10~200Å .

4. The method of claim 1, wherein a thickness of said dielectric film is about 20~2000Å .

5. The method of claim 1, wherein under the metal-insulator-metal capacitor, an underlying layer is formed which includes at least one patterned or unpatterned microelectronic layer with metal lines, dielectric lines and/or microelectric components.

6. A method for forming a polysilicon-insulator-ploysilicon capacitor comprising the steps of:

forming a first polysilicon film and an dielectric film on a semiconductor substrate;

patterning the dielectric film to form a trench through which the first polysilicon film is exposed;

forming an insulation film and a second polysilicon film on a surface of the trench and the dielectric film;

providing a mask pattern defining a capacitor forming area on the second polysilicon film;

forming an upper electrode by etching the second polysilicon film and the insulation film by using the mask pattern and the dielectric film as an etching barrier and an etching stopper layer, respectively;

removing the mask pattern; and

forming a lower electrode by patterning the dielectric film and the first polysilicon film.